Modeling and simulation of an OFDM WLAN receiver

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The development of low-cost and low-power transceivers is indispensable for the realization of today's wireless applications such as wireless local area networks (WLANs), GSM, digital enhanced cordless telecommunications (DECT) and GPS. This however requires a tight integration of the physical layer, which consists of the radio front-end and the DSP-part. Front-ends of telecom transceivers contain functions that are implemented partially in the analog and partially in the digital domain. For an optimal performance of the complete transceiver, it is important that the different domains (digital hardware, software, and analog circuits) are co-designed to some extent. Therefore, tradeoffs between analog and digital systems need to be studied, which requires support from accurate and efficient tools allowing the description and co-simulation of the different building blocks. This demand is quite challenging, since existing simulation tools, employing, e.g. simulation at the transistor level, are not feasible to this end. The use of full-system level simulations is discouraged as well, because of their poor modeling support - their low simulation efficiency for mixed-signal architectures - or their shortcomings towards digital implementation. In addition, modeling complexity should be reduced as much as possible in order to save simulation effort and time.

For the simulation of complete transceiver front-ends, IMEC favors the use of high-level (also known as behavioral level) simulation, which, offering a largely more accurate yet still efficient system model to the system architect, can significantly increase the design productivity. The use of such models is justified by the increasing complexity of the transceiver and by the necessity to come to bit-error-rate (BER) simulations in acceptable CPU times. These BER simulations can be used to test the effectiveness of the trade-offs between the analog and the digital blocks. IMEC presents a high-level approach that enables the joint exploration, simulation, and modeling of the analog and digital part of the receiver in an efficient way. This modeling is based on the coupling of two tightly linked in-house design tools, FAST and OCAPI, whose ingredients were optimized for analog modeling on one side and digital data and control processing on the other side. The effectiveness of the approach is illustrated with a high-level simulation of a WLAN end-to-end link.

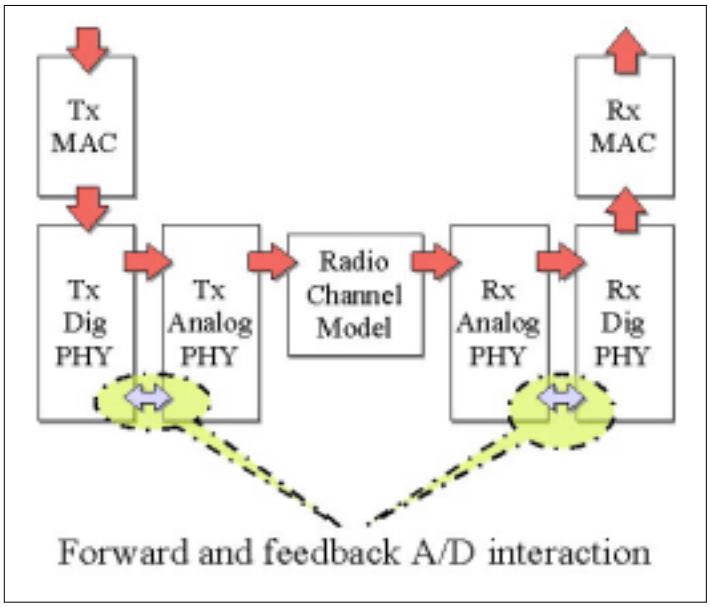

Figure 2: Schematic representation of the WLAN end-to-end link.

Co-simulation with FAST and OCAPI

IMEC's heterogeneous methodology for the modeling, exploration, and simulation of communication transceivers fully integrates digital and analog components into a system model applying dataflow process networks. In addition, it addresses the specific needs on signal processing granularity for the analog parts and datapath/control co-simulation for the digital parts. The method is based on the coupling of two existing C++-based tools: FAST, a high-level, multi-rate, multi-carrier dataflow simulator for analog systems, and OCAPI, the FAST counterpart in the digital domain.

- FAST for analog systems
  IMEC's program FAST is in essence a dataflow simulator. FAST uses a local multi-rate, multi-carrier (MRMC) representation of signals. Each signal in a front-end is considered as a set of one or more modulated carriers, which are each represented with a complex low-pass model and with a - possibly different - time step. The carriers are used locally, meaning that carriers that are important at some place in the architecture are no longer considered at places where they are negligible. The program takes into account harmonics and out-of-band modulations by explicitly addressing them as individual signals. This is important for the simulation of analog systems that cover a large range of frequencies and contain baseband signals around dc.

Next, all linear transfer functions, e.g. represented by s-parameters, that occur in the ana-

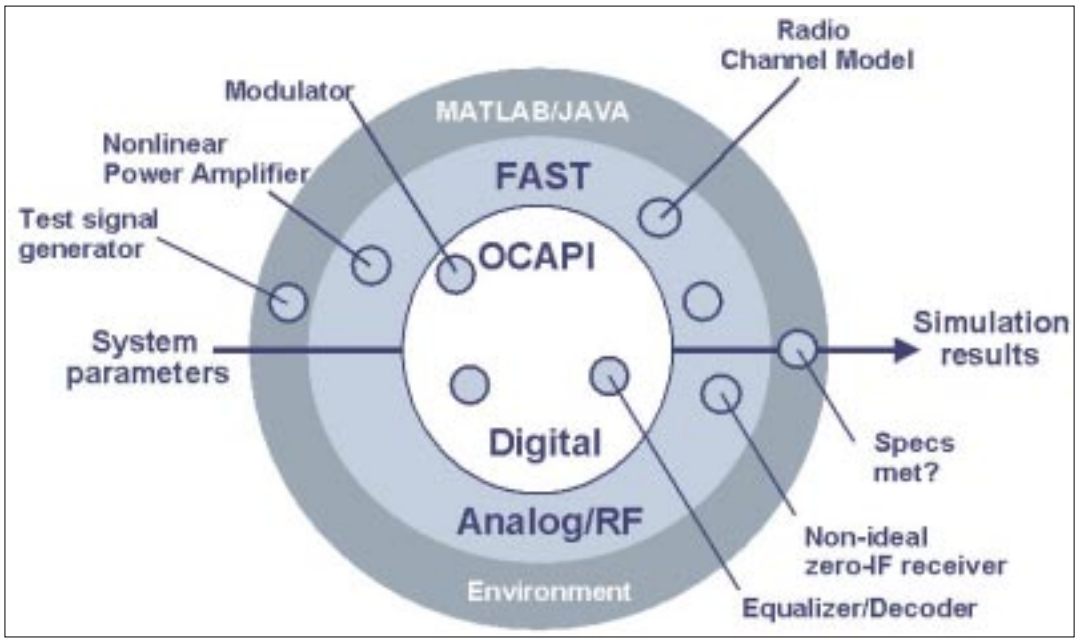

Figure 1: FAST and OCAPI allow efficient modeling and exploration of mixed-signal architectures. FAST contributes its modeling and simulation strength, OCAPI its flexibility and path to implementation.

log models are translated into digital filters prior to the actual simulation. This results in a computational graph consisting of operations such as filtering, rate transformations, time/frequency transformations and summations. These operations can efficiently be implemented by using the FAST kernel library.

This flexible signal description in FAST allows the efficient simulation of low-frequency analog circuits together with RF circuits in one simulation.

- OCAPI for digital systems
  Flexibility in data models, the order of model refinement steps and a path towards HDL code generation are important properties of digital system simulators. IMEC's simulation environment OCAPI serves these digital requirements. It supports gradual refinement of an object-oriented C++ model of a digital system starting from a behavioral dataflow model towards a synthesizable register-transfer level (RTL) description. The RTL consists of a combination of finite state machines and datapaths (FSMD). As such, OCAPI supports mixed simulation of dataflow and RTL models.

- The coupled FAST-OCAPI environment
  IMEC's mixed-signal receiver model originates from the coupling of FAST and OCAPI. At this point, two roads can be taken. (1) Co-simulation can be performed with a common co-simulation backplane or (2) true mixed-signal simulation can be carried out using a single kernel. IMEC decided for keeping separate FAST and OCAPI domains since they differ strongly in functional granularity. This way the environment can also better serve the two traditionally separate designer communities, which are used to different description styles. The interaction between the two domains is only a fraction of the overall dataflow communication. An interfacing layer couples the kernels of FAST and OCAPI, which both use dataflow scheduling. The FAST scheduler is granted master control over the OCAPI schedulers, since it controls a significantly higher number of fine-grain objects. The exchange of data is straightforward, since both simulators implement C++ as data type primitive.

Modeling of the system under test

The benefits of this co-simulation approach have been illustrated using a WLAN end-to-end link as a system under test. This end-to-end link consists of a mixed-signal transmitter and receiver. The radio channel model in between provides it signal to the receiver, which is based on a zero-IF topology and a digital OFDM baseband demodulator. The receive chain starts with an RF section containing a low-noise amplifier (LNA), controllable RF variable gain amplifiers (VGAs) and filters, providing an RF section to a pair of direct down-conversion mixers. After filtering and amplification, the down-converted signals are digitized in A/D converters. Incoming packets are detected by dedicated automatic gain control and dc offset compensation (AGC/DCO) and synchronization. After transformation of the signal into a multi-carrier frequency domain spectrum and subsequent equalization, payload is extracted and passed on to the outer receiver and the MAC.

Prior to simulation, accurate high-level models are required for the analog and mixed-signal blocks, i.e. the RF receiver section and the AGC control loop. These models should cover the relevant signal degrading effects, while, at the same time, they should not be too complex in order to save simulation efforts as much as possible.

IMEC has developed a behavioral RF VGA model and has integrated this into a model of the entire RF section. From the receive-signal perspective, VGAs represent a time-varying system. So far, modeling has been limited to either the nonlinear aspect, the frequency-selectivity or to the feedback loop control. However, IMEC's modeling of a nonlinear VGA including its frequency-dependent 3-port representation characterized by s-parameters and the digital control loop, hence taking all relevant characteristics into account at the same time, is novel. In addition, model complexity from a full time-variant model is reduced down to a switched time-discrete approach through a common look at the analog and the digital side. The VGA model is part of the entire RF receiver model. The RF section, in between the antenna and the down-conversion mixer, is represented by a cascade of the LNA, the filter and the RF VGA. The multi-rate multi-carrier (MRMC) model in FAST allows an efficient description of the entire front-end chain including the switched time-discrete VGA.

To model the mixed-signal automatic gain control loop, IMEC proposes a digital architecture that allows crossing the analog/digital boundary in both directions and that generates timing parameters such as loop delay.

The efforts have resulted in an efficient behavioral mixed-signal model including effects such as frequency selective s-

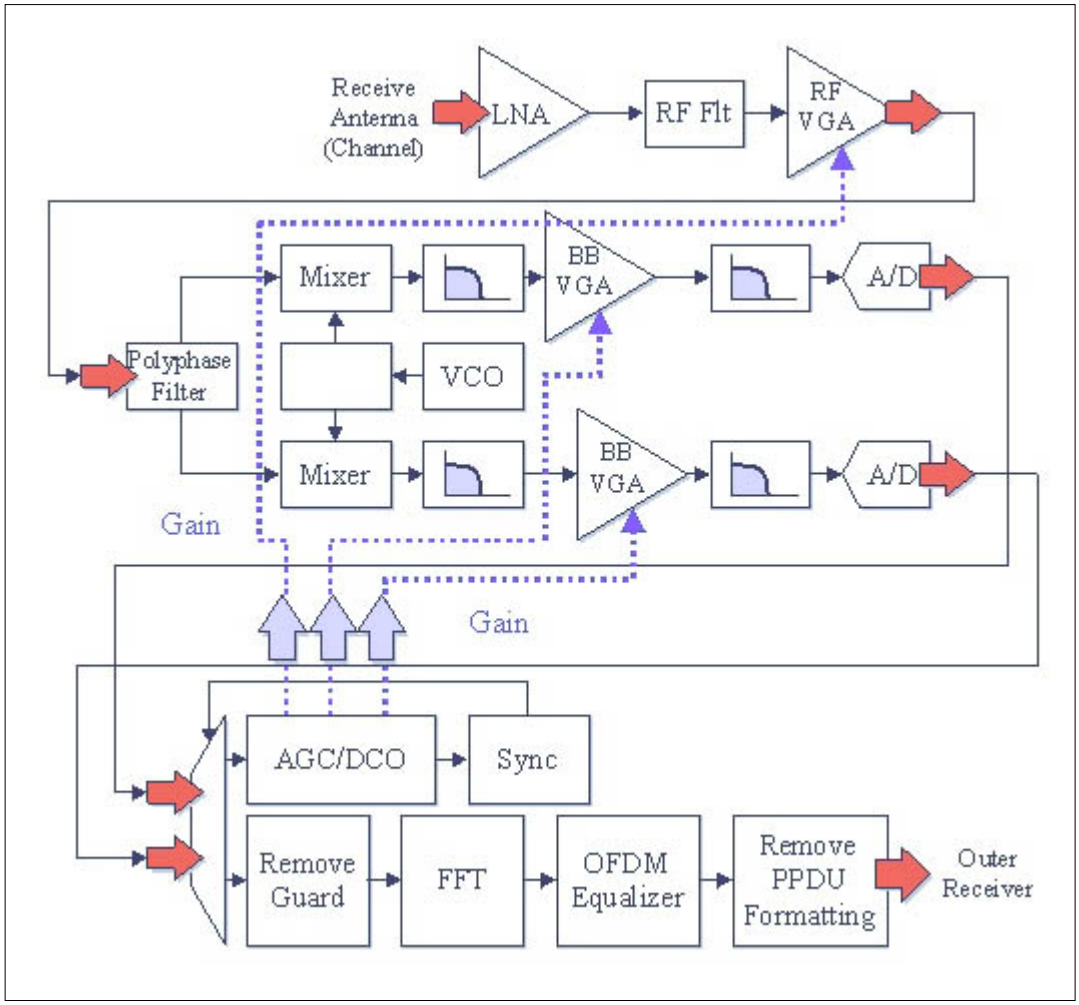

Figure 3: The receive chain.

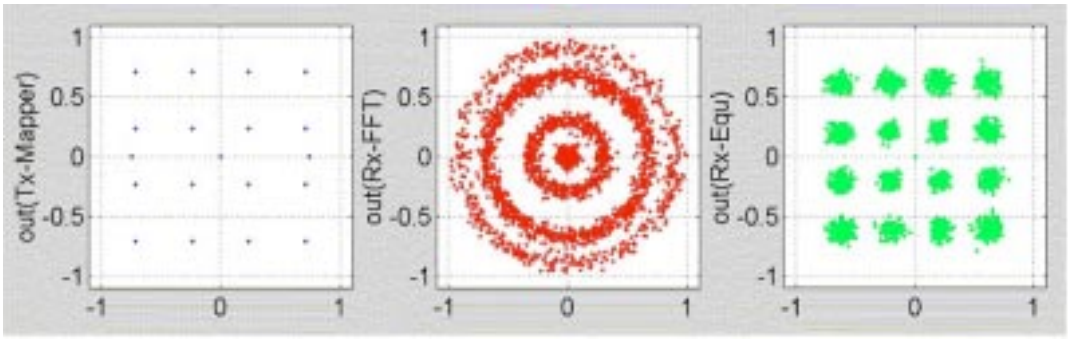

Figure 4: Constellation plots for the mapper (Tx), before equalization (Rx–FFT), and after equalization.

parameters, time-variance, nonlinearities and the entire analog/digital feedback loop. At the same time, the front-end modeling complexity is reduced to a minimum required by the digital processing: its steady-state responses and a 'worst-case' behavior. This simplification allows a very fast yet sufficiently accurate simulation regarding the system functionality.

Simulation results

To prove the applicability and efficiency of IMEC's approach, two cases of design exploration tasks have been selected - both questions that a system designer will ask about a WLAN receiver. The first question is related to end-to-end bit-error-rate (BER) evaluation, commonly used as a measure for the performance of the complete telecom link. With the full transmit/channel/receive end-to-end simulation, the BER of the WLAN link for 80,000 payload bits is determined in about 25s on a Pentium III with 512MB RAM, including all pre-and post-processing. The results can be immediately translated into figures, which show all relevant design information.

A second case concerns a mixed-signal optimization problem around the VGA. The full model allows gain range optimization of the VGA, by enabling the verification of the actual receive range of the receiver in detail and by revealing saturation and noise effects.

Conclusions

IMEC has demonstrated how a joint view at the analog and the digital parts translates into a modeling and simulation approach adapted to the analog, the digital, and the system designer's needs. An efficient behavioral mixed-signal model and a reduction of the front-end modeling complexity have enabled very fast yet accurate enough simulation of an OFDM WLAN receiver. The actual simulation is performed using FAST/OCAPI C++ code.

The example of the OFDM WLAN receiver clearly illustrates how IMEC's methodology and tools support the designer in taking adequate system and architecture decisions during the exploration phase and finally in verifying system performance and functionality during the design refinement phase. They form an interesting suite of tools for advanced architectural studies of mixed-signal telecom systems. More importantly, our scalable modeling approach together with the underlying generic signal description in the FAST simulation kernel is not limited to applications in the WLAN domain. Ongoing research on 4G wireless systems will employ software-defined radio functions and multimode operation, requiring adjustable front-end performance at low cost and power consumption. This requires optimum system exploration at design-time and strong interaction between the analog and digital domain during operation, stressing the need for adequate mixed-signal modeling and simulation methodologies along with a supporting tool chain. □